[0011] In another embodiment of the present invention, multiple parallel conductive lines are placed along side the interconnect. By changing the number of the multiple parallel conductive lines to which the bias voltage is applied, the total capacitance coupled to the interconnect can be adjusted.

[0012] The present invention will be more fully understood in view of the following description and drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0013] Figs. 1A-1C are cross-sectional diagrams of conventional IC capacitive structures;

[0014] Figs. 2A and 2B are circuit diagrams of capacitive structures in accordance with the present invention;

[0015] Fig. 2C is a circuit diagram of an equivalent circuit to a capacitive structure in accordance with the present invention;

[0016] Fig. 2D is an isometric diagram depicting factors affecting the capacitance value of a capacitive structure in accordance with the present invention;

[0017] Figs. 3A-3C are circuit diagrams of capacitive structures in accordance with the present invention; and

[0018] Figs. 4A-4C are circuit diagrams of adjustable capacitive structures in accordance with the present invention.

DETAILED DESCRIPTION OF THE DRAWINGS

[0019] Fig. 2A shows a circuit comprising a capacitive structure 200 in accordance with an embodiment of the present invention. Capacitive structure 200 comprises a conductive line 202 coupled to a bias control circuit 260. Conductive line 202 is positioned parallel to an interconnect 216 that electrically couples a first integrated circuit (IC) device 212 and a second IC device 214 in a single integrated circuit. Bias control circuit 260 comprises circuitry to